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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,640	05/02/2006	Toshihide Tsubata	70404.90/ma	3891

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EXAMINER	
TAYLOR, EARL N	
ART UNIT	**PAPER NUMBER**
2818	

NOTIFICATION DATE	DELIVERY MODE
02/05/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/595,640	TSUBATA ET AL.	
	Examiner	Art Unit	
	EARL N. TAYLOR	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/23/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 21 November 2007 have been fully considered but they are not persuasive. The applicant states "similar to the present invention, the gate insulating film 3 and the semiconductor film 4 are formed in that order after the reaction chamber is cleaned, such that the semiconductor film 4 of Shimizu is disposed on the gate insulating film 3. Since the gate insulating film 3 of Shimizu is formed first, the fluorine remaining in the reaction chamber after cleaning is caught in the gate insulating film 3, not in the semiconductor film 4." The applicant appears to state that fluorine is inherently produced in a cleaning step of the CVD chamber. Shimizu does not do this cleaning step and therefore no fluorine is produced. The applicant is invited to specifically point out in the disclosure of the Shimizu reference where this cleaning step occurs.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 23 January 2008. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 USC § 102 / 103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 102(b) as anticipated by Shimizu (U.S. Patent 5,834,345) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Shimizu (U.S. Patent 5,834,345) in view of Robertson (EP 1154036A1).

Referring to Claim 1, Shimizu teaches a transistor comprising: a source electrode and a drain electrode (7 and 8) arranged in mutually opposing relation; a semiconductor film comprising at least one layer (4) disposed between the source electrode and the drain electrode (7 and 8); a gate electrode (2) disposed in adjacent relation to the semiconductor film (4); and a gate insulating film (3) disposed between the gate electrode (2) and each of the source electrode, the drain electrode, (7 and 8) and the semiconductor film (4), the transistor is of an inverted stagger type in which the gate insulating film (3) and the semiconductor film (4) are formed in that order and the

semiconductor film (4) is disposed on the gate insulating film (3); and the gate insulating film (3) is an amorphous silicon nitride film (Col. 3, Lines 55-65); wherein gate insulating film (3) does not contain a concentration of fluorine, meaning the concentration of fluorine is zero because no cleaning step using fluorine is performed which anticipates the range of 1 x 10^{20} atoms/cm^3 or less and the range of 1 x 10^{19} atoms/cm^3 or less.

Assuming *arguendo*, if one were to interpret the reference so narrowly such that a cleaning step producing fluorine residue or particulates in the subsequent CVD of the amorphous silicon nitride gate insulating film is inherent as argued in applicant's remarks filed on 21 November 2007 at page 5, last paragraph it would be rejected as unpatentable over Shimizu in view of Robertson et al. (EP 1154036 A1). Shimizu teaches a transistor comprising: a source electrode and a drain electrode (7 and 8) arranged in mutually opposing relation; a semiconductor film comprising at least one layer (4) disposed between the source electrode and the drain electrode (7 and 8); a gate electrode (2) disposed in adjacent relation to the semiconductor film (4); and a gate insulating film (3) disposed between the gate electrode (2) and each of the source electrode, the drain electrode, (7 and 8) and the semiconductor film (4), the transistor is of an inverted stagger type in which the gate insulating film (3) and the semiconductor film (4) are formed in that order and the semiconductor film (4) is disposed on the gate insulating film (3); and the gate insulating film (3) is an amorphous silicon nitride film (Col. 3, Lines 55-65); but does not teach wherein a cleaning step is performed using fluorine and then the fluorine residue and particulates are removed such that the gate insulating film (3) does not contain a concentration of fluorine or that the concentration

of fluorine is 1 x 10^{20} atoms/cm^3 or less or 1 x 10^{19} atoms/cm^3 or less. Robertson teaches cleaning the CVD chamber using fluorine and thereafter completely removing fluorine residue and particulates from the CVD chamber (par. 5-11 and 23). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to clean the CVD apparatus of Shimizu with the method taught by Robertson thus removing fluorine from being present in the amorphous silicon nitride in order to prevent the threshold of devices from shifting and to prevent substrate damage (par. 5-11 and 23).

Referring to Claim 3, Shimizu further teaches wherein the transistor is of a field-effect type (Col. 1, Lines 6-10).

Referring to Claim 5, Shimizu teaches all of the limitations of Claim 1, wherein the gate insulating film (3) is deposited by a CVD method (Col. 3, Lines 55-65). Furthermore, the language, term, or phrase "the gate insulating film is deposited by a CVD method", is directed towards the process of of depositing a film. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new

method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the claim language only requires a gate insulating film, which does not distinguish the invention from Shimizu, who teaches the structure as claimed.

Referring to Claim 8, Shimizu teaches all of the limitations of Claim 1 wherein a liquid crystal display device comprising the transistor of claim 1 as a switching element for a pixel electrode portion (Col. 1, Lines 6-10).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Telephone / Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Earl N. Taylor whose telephone number is (571) 272-8894. The examiner can normally be reached on Monday-Friday from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Earl N. Taylor

DAVID VU
PRIMARY EXAMINER